DATA SHEET

TDA1545A
Stereo continuous calibration DAC

Preliminary specification
File under Integrated Circuits, IC01

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Philips
Semiconductors

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FEATURES

- Space saving package (SO8 or DIL8)
- Low power consumption
- Low total harmonic distortion
- Wide dynamic range (16-bit resolution)
- Continuous calibration concept
- Easy application: single 3 to 5.5 V rail power supply and output- and bias current are proportional to the supply voltage
- Fast settling time permits 2 ×, 4 × and 8 × oversampling (serial input) or double speed operation at 4 × oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range of –40 °C to +85 °C
- Compatible with most of the Japanese input formats: time multiplexed, two's complement and TTL
- No zero crossing distortion.

GENERAL DESCRIPTION

The TDA1545A is the first device of a new generation of the digital-to-analog convertors which embodies the innovative technique of continuous calibration. The largest bit-currents are repeatedly generated by one single current reference source. This duplication is based upon an internal charge storage principle having an accuracy insensitive to ageing, temperature and process variations.

The device is fabricated in a 1.0 µm CMOS process and features an extremely low power dissipation, small package size and easy application. Furthermore, the accuracy of the high coarse current combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensures high quality audio reproduction. Therefore, the continuous calibration digital-to-analog convertor is eminently suitable for use in (portable) digital audio equipment.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1545A(1)	8	DIL	plastic	SOT97
TDA1545AT(2)	8	mini-pack	plastic	SO8; SOT96A

Notes

1. SOT97-1; 1996 August 19.
2. SOT96-1; 1996 August 19.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3	5	5.5	V
I_{DD}	supply current	V_{DD} = 5 V; at code 0000H	–	3.0	4.0	mA
I_{FS}	full scale output current					
		V_{DD} = 5 V	0.9	1.0	1.1	mA
		V_{DD} = 3 V	–	0.6	–	mA
THD	total harmonic distortion	including noise				
		at 0 dB	–	–88	–78	dB
		at 0 dB	–	0.004	0.01	%
		at –60 dB	–	–33	–24	dB
		at –60 dB	–	2.2	6	%
		at –60 dB; A-weighting	–	–35	–	dB
		at –60 dB; A-weighting	–	1.7	–	%
		at –60 dB; A-weighting; R3 = R4 = 11 kΩ; I_{FS} = 2 mA	–	1.4	–	%
S/N	signal-to-noise ratio at bipolar zero					
		A-weighting; at code 0000H	86	98	–	dB
		R3 = R4 = 11 kΩ; I_{FS} = 2 mA	–	101	–	dB
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
BR	input bit rate at data input		–	–	18.4	Mbits/s
f_{BCK}	clock frequency at clock input		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (IOL; IOR)		–	±400	–	ppm
P_{tot}	total power dissipation	at code 0000H				
		V_{DD} = 5 V	–	15	20	mW
		V_{DD} = 3 V	–	6	–	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C

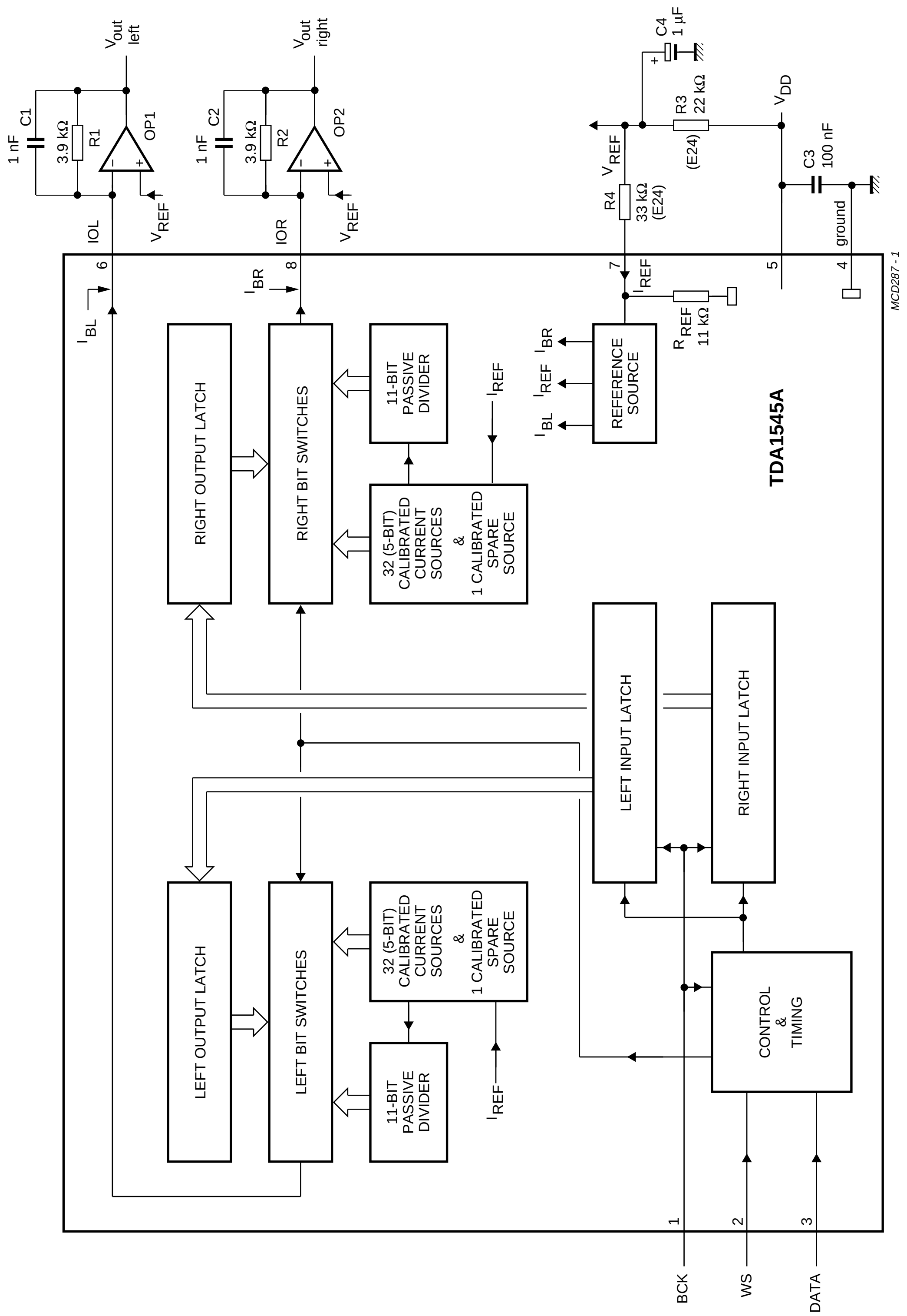


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	positive supply voltage
IOL	6	left channel output
I_{REF}	7	reference current input
IOR	8	right channel output

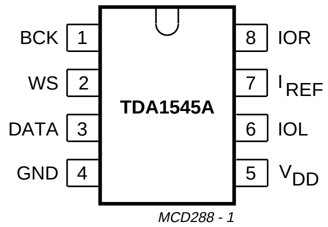


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig.3. The figure shows the calibration principle (Fig.3a) and operation principle (Fig.3b). During calibration of the MOS current source (Fig.3a) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After calibration of the drain current to the reference value I_{REF}, the switch S1 is opened and S2 is switched to the other position (Fig.3b). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore the drain current of M1 will still be equal to I_{REF} and this exact duplicate of I_{REF} is now available at the I_{out} terminal. The 32 current sources and the spare current source of the TDA1545A are continuously calibrated (see Fig.1). The spare current is included to allow for continuous convertor operation. The output of one calibrated source is connected to an 11-bit binary current divider consisting of 2048 transistors. A symmetrical offset decoding principle is incorporated and arranges the bit switching in such a way that the zero-crossing is performed only by the LSB currents.

The TDA1545A accepts input serial data formats of 16-bit word length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5. With a LOW level on the word select input (WS) input data is placed in the right input register and with a HIGH level on the WS input data is placed in the left input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.
An internal bias current I_{bias} (see IBL and IBR in Fig.1) is added to the full scale output current IFS in order to achieve the maximum dynamic range at the outputs of OP1 and OP2 (see Fig.1). The reference input current IREF controls with gain AFS the current IFS which is a sink current and with gain Abias the I_{bias} which is a source current (note 1). The current I_{REF} is proportional to V_{DD} so the I_{FS} and I_{bias} will also be proportional to V_{DD} (note 2) because A_{FS} and A_{bias} are constant. The reference output voltage V_{REF} in Fig.1 is $\frac{2}{3}$ V_{DD}. In this way the maximum dynamic range is achieved over the entire power supply range. The tolerance of the reference input current in Fig.1 depends on the tolerance of the resistors R3, R4 and R_{REF} (note 3).

Notes to the functional description

1. $I_{FS} = A_{FS} \times I_{REF}$ and $I_{bias} = A_{bias} \times I_{REF}$
2. $\frac{V_{DD1}}{V_{DD2}} = \frac{I_{FS1}}{I_{FS2}} = \frac{I_{bias1}}{I_{bias2}}$
3. $\Delta I_{REF} = I_{REF} - \frac{V_{DD}}{R3 + \Delta R3 + R4 + \Delta R4 + R_{REF} + \Delta R_{REF}}$

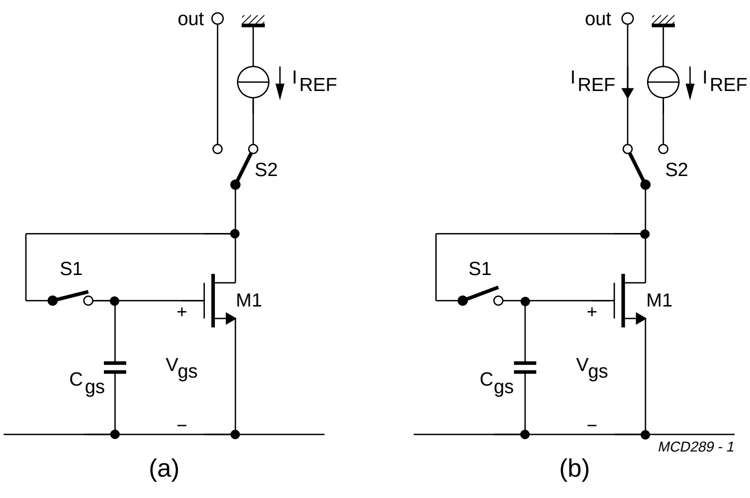


Fig.3 Calibration principle; (a) calibration, (b) operation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	–	6	V
T_{XTAL}	maximum crystal temperature	–	+150	°C
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	–40	+85	°C
V_{es}	electrostatic handling (note 1)	–2000	+2000	V
V_{es}	electrostatic handling (note 2)	–200	+200	V

Notes

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
2. Machine model; C = 200 pF, L = 0.5 µH, R = 10 Ω, 3 zaps positive and negative.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT97	100 K/W
	SOT96A	210 K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; measured in the circuit of Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	note 1	–	3.0	4.0	mA
RR	ripple rejection	note 2	–	30	–	dB
Digital inputs (WS; BCK; DATA)						
$\|I_{IL}\|$	input leakage current LOW	V_I = 0.8 V	–	–	10	µA
$\|I_{IH}\|$	input leakage current HIGH	V_I = 2.4 V	–	–	10	µA
f_{BCK}	bit clock input frequency		–	–	18.4	MHz
BR	bit rate data input		–	–	18.4	Mbits/s
f_{WS}	word select input		–	–	384	kHz
Timing (Fig.4)						
t_r	rise time		–	–	12	ns
t_f	fall time		–	–	12	ns
t_{CY}	bit clock cycle time		54	–	–	ns
t_{HB}	bit clock HIGH time		15	–	–	ns
t_{LB}	bit clock LOW time		15	–	–	ns
$t_{SU;DAT}$	data set-up time		12	–	–	ns
$t_{HD;DAT}$	data hold time		2	–	–	ns
$t_{HD;WS}$	word select hold time		2	–	–	ns
$t_{SU;WS}$	word select set-up time		12	–	–	ns
Analog input (I_{REF})						
R_{REF}	reference resistor (Fig.1)		7.4	11.0	14.6	kΩ
Analog outputs (IOL; IOR)						
Res	resolution		–	–	16	bit
V_{DCC}	DC output voltage compliance		2.0	–	V_{DD}–1	V
I_{FS}	full scale current		0.9	1.0	1.1	mA
T_{CFS}	full scale temperature coefficient		–	±400	–	ppm
I_{bias}	bias current		643	714	785	µA
A_{FS}	reference input current to full scale output current gain		–	13.2	–	
A_{bias}	reference input current to bias current gain		–	9.42	–	
THD	total harmonic distortion	including noise at 0 dB; note 3, see Fig.6	– –	–88 0.004	–78 0.01	dB %
THD	total harmonic distortion	including noise at –60 dB; note 3, Fig.6	– –	–33 2.2	–24 6	dB %

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	including noise at –60 dB,	–	–35	–	dB
		A-weigthing	–	1.8	–	%
		R3 = R4 = 11 kΩ see Fig.1; I_{FS} = 2 mA	–	1.4	–	%
THD	total harmonic distortion	including noise at 0 dB; note 4	–	–84	–70	dB
			–	0.006	0.03	%
t_{cs}	settling time ± 1 LSB		–	0.2	–	μs
α	channel separation		86	95	–	dB
$\|d_{IO}\|$	unbalance between outputs	note 3	–	0.2	0.3	dB
$\|t_d\|$	delay time between outputs		–	±0.2	–	μs
S/N	signal-to-noise ratio (A-weighting)	at bipolar zero; note 1	86	98	–	dB
S/N	signal-to-noise ratio (A-weighting)	at bipolar zero; note 5	–	101	–	dB

Notes

1. At code 0000H.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz sinewave over a 20 Hz to 20 kHz bandwidth generated at a sampling rate of 192 kHz.
5. R3 = R4 = 11 kΩ; see Fig.1; I_{FS} = 2 mA.

TEST AND APPLICATION INFORMATION

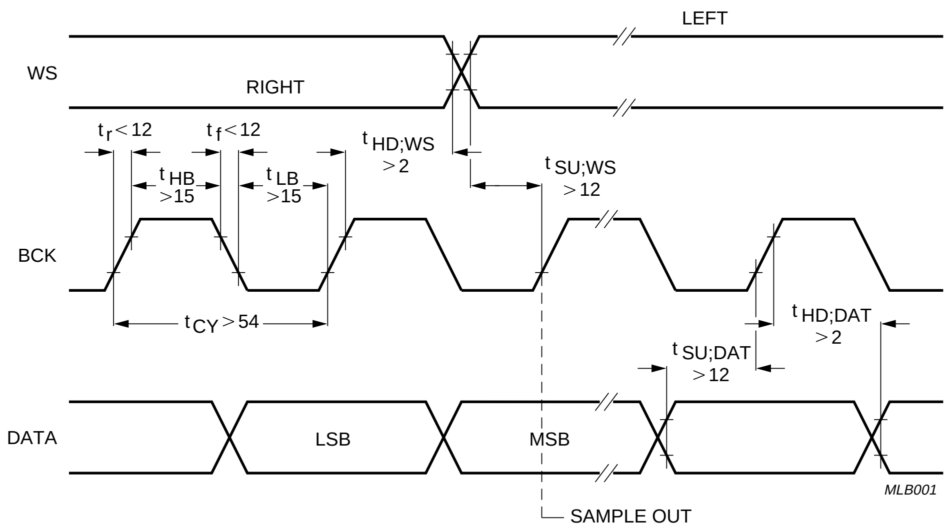


Fig.4 Timing and input signals.

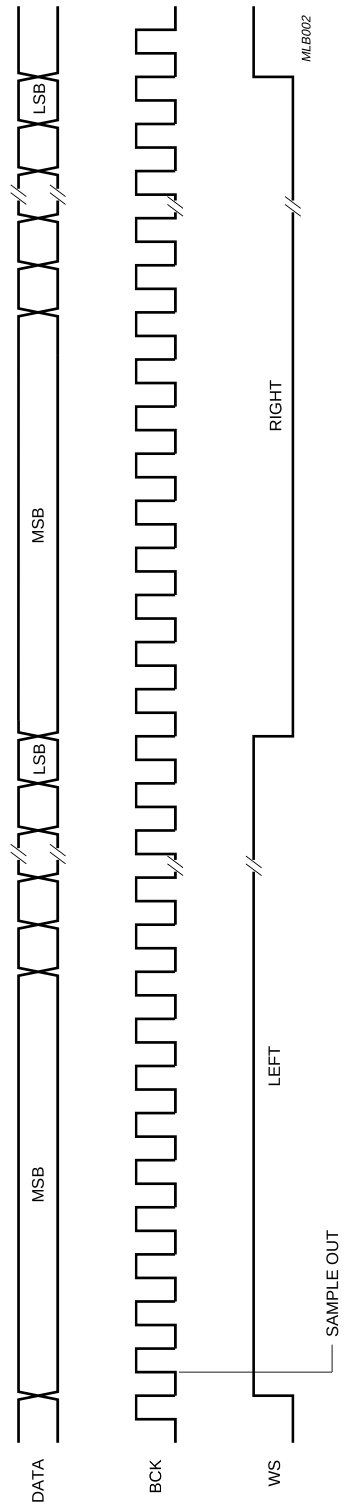
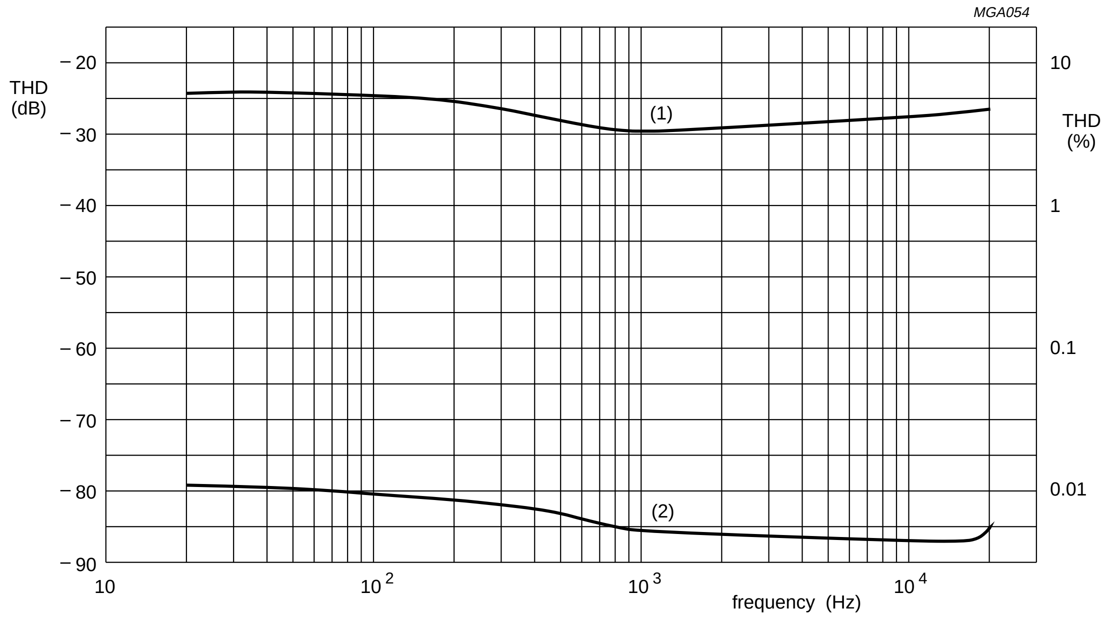


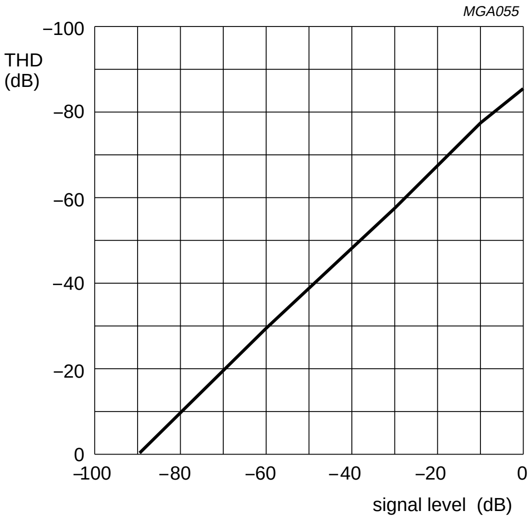
Fig.5 Format of input signals.

APPLICATION INFORMATION



(1) Measured including all distortion plus noise at a level of −60 dB
(2) Measured including all distortion plus noise at a level of −0 dB
The sample frequency 4FS: 176.4 kHz
The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied

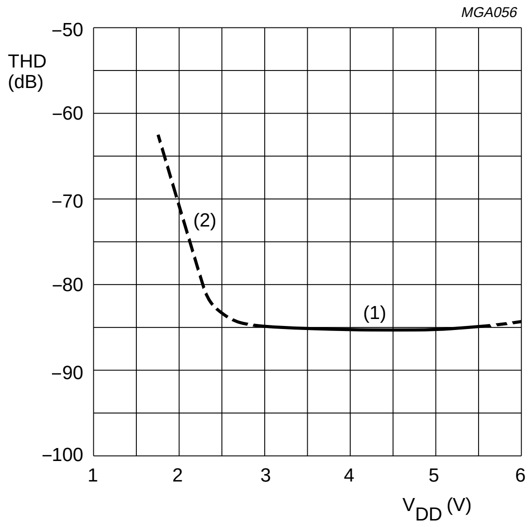
Fig.6 Total harmonic distortion as a function of frequency (4FS).



The sample frequency 4FS: 176.4 kHz

The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied

Fig.7 Total harmonic distortion as a function of signal level (4FS).



(1) Measured within the specified operating supply voltage range

(2) Measured outside the specified operating supply voltage range

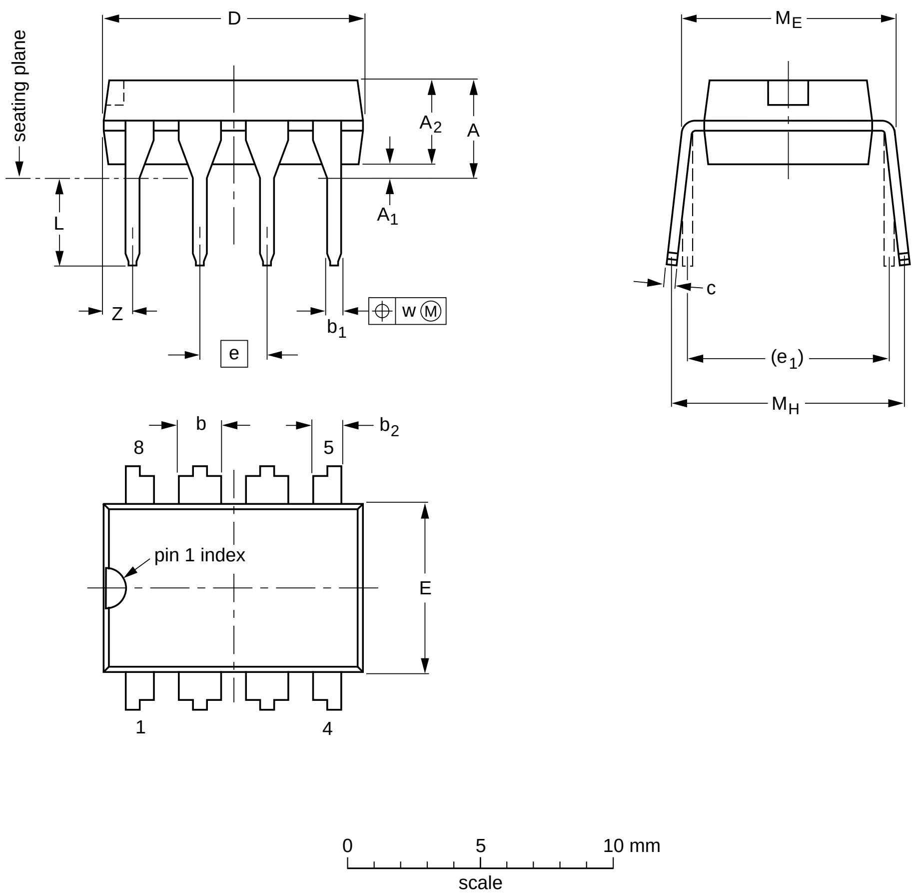
The sample frequency 4FS: 176.4 kHz

The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied

Fig.8 Total harmonic distortion as a function of supply voltage V_{DD} (4FS).

PACKAGE OUTLINES

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

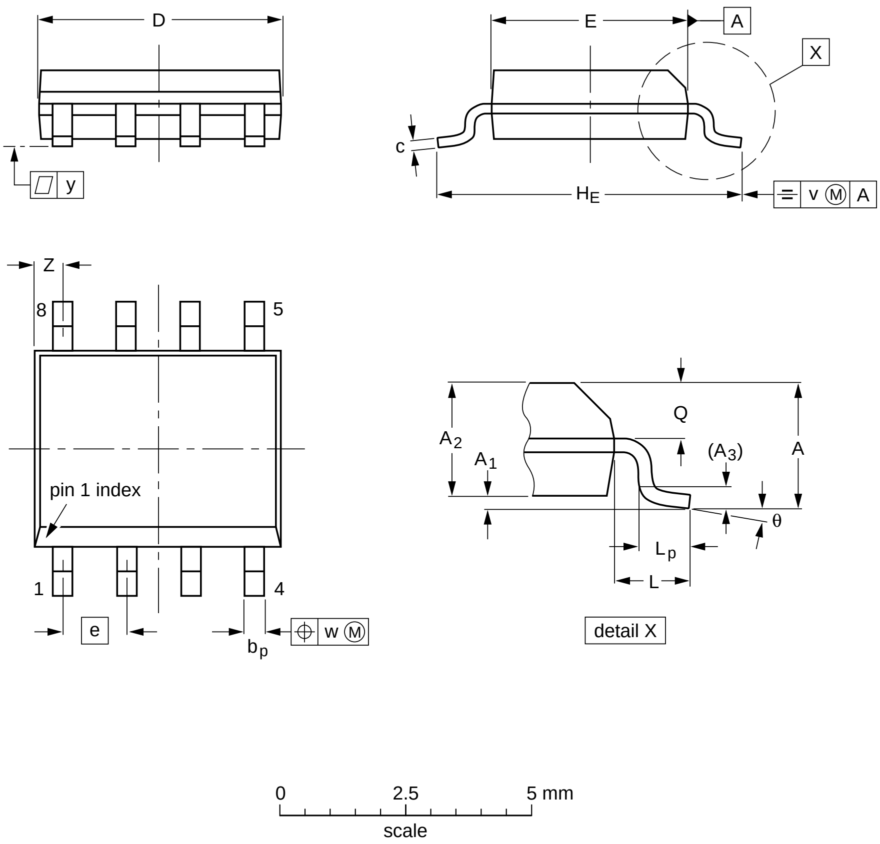
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.